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10/772,431	02/06/2004	Mitsuharu Tai	NITT.0188	8944

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EXAMINER	
VU, PHU	

ART UNIT	PAPER NUMBER
2871	

DATE MAILED: 08/09/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/772,431	TAI ET AL.	
	Examiner	Art Unit	
	Phu Vu	2871	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 1-12 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 1-12 is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claim 1 is rejected under 35 U.S.C. 102(b) as being anticipated by Tanaka et al US Patent No 5851440.

Regarding claim 1, Tanaka discloses an image display device provided with an active-matrix substrate comprising: an insulating substrate (fig. 1 element 10); and a plurality of circuit regions fabricated on said insulating substrate and including at least a pixel section and a pixel driving circuit section each of said pixel section and said pixel-driving circuit section having a polycrystalline silicon semiconductor film, wherein at least one of said plurality of circuit regions has a first type of a thin film transistor (T1) and a second type of a thin film transistor (T2), and a direction of current flowing through a channel of said first type of a thin film transistor is different from that of a current flowing through a channel of said second type thin film transistor (see abstract). The reference discloses monopolar TFTs and bipolar TFTs driving various portions of the display. Bipolar TFTs allow current to flow from drain to the source in positive mode and in negatively biased mode the current flows from the source to the drain. Monopolar only allows flow in 1 direction. See column 2 lines 13-63.

Regarding claim 2, Tanaka teaches an image display device provided with an active-matrix substrate comprising: an insulating substrate (fig. 1 element 10); and a plurality of circuit regions fabricated on said insulating substrate and including at least a pixel section and a pixel-driving circuit section, each of said pixel section and said pixel-driving circuit section having a polycrystalline silicon semiconductor film, wherein said plurality of circuit regions includes at least one pair of a first circuit region and a second circuit region, all thin film transistors in said first circuit region flow currents through channels thereof in a first direction, all thin film transistors in said second circuit region flow currents through channels thereof in a second direction, and said first direction is different from said second direction as indicated by claim 1 rejection the reference discloses forming bipolar and monopolar TFTs in regions therefore the first region is considered as a region where there is a bipolar TFT and the second region is the region where there is a monopolar TFT thus the direction of currents will be different for each region and the same within a region.

Regarding claim 3, An image display device according to claim 1, wherein said plurality of circuit regions includes at least one pair of a first-type circuit region and a second-type circuit region, all thin film transistors in said first-type circuit region flow currents through channels thereof in one direction, and directions of currents flowing through channels of thin film transistors in said second-type circuit region are plural in number claim 1 rejection the reference discloses forming bipolar and monopolar TFTs in regions therefore the first region is considered as a region where there is a bipolar TFT

and the second region is the region where there is a monopolar TFT thus the direction of currents will be different for each region and the same within a region.

Regarding claim 4, an image display device according to claim 3, wherein said one direction is same in all of said first-type circuit regions included in said plurality of circuit regions. The reference disclosed monopolar TFTs where current only flows in one direction (see claim 1 rejection) therefore this region all the currents will flow in the same direction.

Regarding claim 7, the reference shows an image display device according to claim 1, wherein said thin film transistors of said first and second types have plural kinds of gate insulating materials and plural kinds of thickness in each of said plurality of circuit regions (see fig. 1 shows varying thickness in each of TFTs T1 and T2 and also see column 11 lines 5 – 27 for various gate insulators).

Regarding claim 8, the reference shows the first and second transistors having plural kinds of structures in each of said circuit regions (see fig. 12 which shows the thin film transistors of the invention placed on a substrate). The reference shows a shift registers (fig. 12 element 21) and side driver circuits (fig. 12 element 52).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 5-6 and 9-12 are rejected under 35 U.S.C. 103(a) as being unpatentable over Tanaka in view of and further in view of Namakura et al US Patent No. 6887724 and further in view of Ogawa US Patent No. 6479837 and further in view of Wada et al. US Patent No. 6673639 and further in view of Yamada et 20020158298 and further in view of Hagino et al US Publication No. 2002/0142567.

Regarding claims 5, and 6 the references teach all the limitations of claims 5 and 6 except an image display device, wherein, in said first-type circuit region, a peak-to-valley height difference of a surface of said channel, a source region and a drain region of said thin film transistors is equal to or smaller than 5 nm, and crystalline grains of said polycrystalline silicon semiconductor film are of a rectangular shape of 0.3 to 2 .microns in width and 4 microns or more in length; and in said second-type circuit region, an average crystalline grain diameter is 1 microns or smaller and a peak-to-valley height difference of a surface is equal to or greater than 20 nm, in said channel, a source region and a drain region of said thin film transistors.

Nakamura discloses an irradiation process for improving crystallinity of crystalline semiconductor films and also has less defects which is provided by a process that also reduces the peak to valley value of the semiconductor to less than 5 nm.

Ogawa discloses a thin film transistor with polycrystalline silicon with a grain size of 3-5 microns in the scanning direction and .5 to 2 microns (column 10 lines 3-13) in the microns in the other direction for high mobility and uniform transistor properties (see column 5 lines 10 – 25). The MPEP states: In the case where the claimed ranges

"overlap or lie inside ranges disclosed by the prior art" a prima facie case of obviousness exists. In re Wertheim, 541 F.2d 257, 191 USPQ 90 (CCPA 1976);

Wada discloses polycrystalline silicon layers large grain sizes of 800 nm (less than 1 micron see fig. 5). Yamada discloses TFTs with a polycrystalline silicon layer with large grain sizes having improved switching speed suitable for driver circuitry.

Hagino discloses a transistor with semiconductor layer having a peak-to-valley height difference of 60 nm with high smoothness and highly reliability (see [0015] and [0031]). Therefore, at the time of the invention, it would have been obvious to one of ordinary skill in the art to use transistors with a peak-to-valley value of less than 5 nm and a grain size of 4 microns or more in length and .3 to 2 microns in width to improve crystallinity, defects, and high mobility and it also would have been obvious to to use a peak to valley height difference of 60 nm and a grain size of less than 1 micron to achieve high reliability and avoid dispersions in mobility. Thus different surface configurations (peak to peak height and grain size) have been shown by the combination of reference.

Regarding claim 9, Tanaka discloses an image display device provided with an active-matrix substrate comprising: an insulating substrate (fig. 1 element 10); and a plurality of circuit regions fabricated on said insulating substrate and including at least a pixel section and a pixel driving circuit section each of said pixel section and said pixel-driving circuit section having a polycrystalline silicon semiconductor film, wherein at least one of said plurality of circuit regions has a first type of a thin film transistor (T1) and a second type of a thin film transistor (T2), and a direction of current flowing

through a channel of said first type of a thin film transistor is different from that of a current flowing through a channel of said second type thin film transistor (see abstract). The reference discloses monopolar TFTs driving the peripheral portions and bipolar TFTs drive the pixel portion. Bipolar TFTs allow current to flow from drain to the source in positive mode and in negatively biased mode the current flows from the source to the drain. Monopolar only allows flow in 1 direction. See column 2 lines 13-63. Nakamura discloses an irradiation process for improving crystallinity of crystalline semiconductor films and also has less defects which is provided by a process that also reduces the peak to valley value of the semiconductor to less than 5 nm.

Ogawa discloses a thin film transistor with polycrystalline silicon with a grain size of 3-5 microns in the scanning direction and .5 to 2 microns (column 10 lines 3-13) in the microns in the other direction for high mobility (300 cm^2 / Vs) and uniform transistor properties (see column 5 lines 10 – 25). In the case where the claimed ranges "overlap or lie inside ranges disclosed by the prior art" a prima facie case of obviousness exists. In re Wertheim, 541 F.2d 257, 191 USPQ 90 (CCPA 1976);

Wada discloses polycrystalline silicon layers large grain sizes of 800 nm (less than 1 micron see fig. 5). Yamada discloses TFTs with a polycrystalline silicon layer with large grain sizes having improved switching speed suitable for driver circuitry.

Hagino discloses a transistor with semiconductor layer having a peak-to-valley height difference of 60 nm with high smoothness and highly reliability (see [0015] and [0031]). Therefore, at the time of the invention, it would have been obvious to one of ordinary skill in the art to use transistors with a peak-to-valley value of less than 5 nm

and a grain size of 4 microns or more in length and .3 to 2 microns in width to improve crystallinity, defects, and high mobility and it also would have been obvious to to use a peak to valley height difference of 60 nm and a grain size of less than 1 micron to achieve high reliability and avoid dispersions in mobility. Thus different surface configurations (peak to peak height and grain size) have been shown by the combination of reference.

Regarding claim 10, the reference shows an image display device according to claim 1, wherein said thin film transistors of said first and second types have plural kinds of gate insulating materials and plural kinds of thickness in each of said plurality of circuit regions (see fig. 1 shows varying thickness in each of TFTs T1 and T2 and also see column 11 lines 5 – 27 for various gate insulators).

Regarding claim 11, the reference shows the first and second transistors having plural kinds of structures in each of said circuit regions such as a source, gate and drain region (see fig. 1) and these transistors constitute the pixel section.

Claim 12 is rejected under 35 U.S.C. 103(a) as being unpatentable over Tanaka in view of and further in view of Namakura and further in view of Ogawa and further in view of Yamaguchi and further in view of Hagino and further in view of Yamada and further in view of Wada and further in view of Shih et al US Publication No. 20040038438.

Regarding claim 12, the primary reference discloses a level shifter, a sampling circuit, and a buffer circuit constituting TFTs (see column 12 lines 23-58). The references disclose all the limitations of claim 12 except the plurality of circuit regions

constituting the pixel section, said channel, said source region and said driving region of said TFTs constituting pixel-driving circuits formed of polycrystalline silicon films having an average grain diameter of 1 micron or smaller and a peak-to-valley height different equal to or greater than 20 nm. However, Yamada and Wada as disclosed in the claim 9 rejection disclosed an average grain diameter of 800 nm which was considered large had attributes that gave transistors fast switching speed ideal for pixel driving circuitry. Shih discloses peak to valley heights are directly related grain size and a leakage current is attributed to large peak-to-valley height (see [0006]). Therefore a peak-to-valley height greater than 20 nm is considered a property of a large grain sizes of 1 micron in diameter. Ogawa as in the claim 9 rejection disclosed a TFT with grains .3 microns to 2 microns in width and 3-5 microns in height having uniform transistor characteristics which creates uniform pixels and Shih discloses a low peak-to-valley height for low leakage current (see [0006]). In the case where the claimed ranges "overlap or lie inside ranges disclosed by the prior art" a prima facie case of obviousness exists. In re Wertheim, 541 F.2d 257, 191 USPQ 90 (CCPA 1976); Shih discloses leakage current is an adverse property for pixels. Therefore, at the time of the invention, it would have been obvious to one of ordinary skill form large grain polycrystalline silicon layer transistors which have a large peak-to-valley value to obtain a high switching speed and it would have been obvious to one of ordinary skill in the art to use transistors with a grain size of .3 to 2 microns in width and 4 or more microns in length with a peak-to-valley value of the polysilicon layer to improve pixel uniformity and reduce leakage current.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Phu Vu whose telephone number is (571)-272-1562. The examiner can normally be reached on 8AM-5PM M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Robert Kim can be reached on (571)-272-2293. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Phu Vu
Examiner
AU 2871

DUNG T. NGUYEN
PRIMARY EXAMINER